EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	76	(switch snoop broadcast) and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/12 14:22
S24	65	"711"/$.ccls. and S23	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/13 14:33
S161	8887	(snoop broadcast (all adj2 nodes)) with (local "same" adj node)	US-PGPUB; USPAT	OR	ON	2006/06/06 18:17
S163	105	(cache directory mode) and S162	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/06 18:42
S164	5	GOTL global adj ownership adj tag adj list	US-PGPUB; USPAT	OR	ON	2006/06/07 12:39
S173	77	coherence adj request	US-PGPUB; USPAT; USOCR	OR	ON	2006/06/07 16:07
S175	69	protocol and S174	US-PGPUB; USPAT; USOCR	OR	ON	2006/06/07 16:07
S178	147	((cypher with (robert bob)) (singhal with ashok)).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/07 17:16
S183	2953	directory and S182	US-PGPUB; USPAT	OR	ON	2006/06/12 14:22
S184	1296	S183 and coheren$3	US-PGPUB; USPAT	OR	ON	2006/06/12 14:22
S191	207	global with coheren$3 and S185	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/13 14:33

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S193	5	"global coherency filter"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/12 14:40
S196	6529	cache with protocol	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/13 14:33
S199	43	S198 and @ad<"20010501"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/13 14:34
S201	15483	shared adj memory	US-PGPUB; USPAT	OR	ON	2006/06/13 14:35
S206	29	(hagersten cypher landin Loewenstein).in. and mode adj2 unit	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/13 15:14

	Document ID	Title	Current OR	Inventor
1	US 6738868 B2	System for minimizing directory information in scalable multiprocessor systems with logically independent input/output nodes	711/141	Gharachorloo; Kourosh et al.
2	US 20020087807 A1	System for minimizing directory information in scalable multiprocessor systems with logically independent input/output nodes	711/141	Gharachorloo, Kourosh et al.
3	US 20010013089 A1	CACHE COHERENCE UNIT FOR INTERCONNECTING MULTIPROCESSOR NODES HAVING PIPELINED SNOOPY PROTOCOL	711/146	WEBER, WOLF-DIETRICH
4	US 6081874 A	Non-uniform memory access (NUMA) data processing system that speculatively issues requests on a node interconnect	711/141	Carpenter; Gary Dale et al.
5	US 6751698 B1	Multiprocessor node controller circuit and method	710/317	Deneroff; Martin M. et al.
6	US 6633958 B1	Multiprocessor computer system and method for maintaining cache coherence utilizing a multi-dimensional cache coherence directory structure	711/141	Passint; Randal S. et al.

	Document ID	Title	Current OR	Inventor
7	US 6578115 B2	Method and apparatus for handling invalidation requests to processors not present in a computer system	711/144	McCracken; David E. et al.
8	US 20020112132 A1	Coherence controller for a multiprocessor system, module, and multiprocessor system wtih a multimodule architecture incorporating such a controller	711/141	Lesmanne, Sylvie et al.
9	US 20020002659 A1	SYSTEM AND METHOD FOR IMPROVING DIRECTORY LOOKUP SPEED	711/141	MICHAEL, MAGED MILAD et al.
10	US 5802582 A	Explicit coherence using split-phase controls	711/152	Ekanadham; Kattamuri et al.
11	US 20020087804 A1	Distributed mechanism for resolving cache coherence conflicts in a multi-node computer architecture	711/141	Khare, Manoj et al.
12	US 6868481 B1	Cache coherence protocol for a multiple bus multiprocessor system	711/119	Gaither; Blain D. et al.
13	US 20030131201 A1	Mechanism for efficiently supporting the full MESI (modified, exclusive, shared, invalid) protocol in a cache coherent multi-node shared memory system	711/144	Khare, Manoj et al.

	Document ID	Title	Current OR	Inventor
14	US 6587930 B1	Method and system for implementing remstat protocol under inclusion and non-inclusion of L1 data in L2 cache to prevent read-read deadlock	711/144	Deshpande; Sanjay Raghunath et al.
15	US 6088769 A	Multiprocessor cache coherence directed by combined local and global tables	711/141	Luick; David Arnold et al.
16	US 5983326 A	Multiprocessing system including an enhanced blocking mechanism for read-to-share-transactions in a NUMA mode	711/147	Hagersten; Erik E. et al.
17	US 7032078 B2	Shared memory multiprocessing system employing mixed broadcast snooping and directory based coherency protocols	711/141	Cypher; Robert et al.
18	US 6973545 B2	System with a directory based coherency protocol and split ownership and access right coherence mechanism	711/141	Cypher; Robert E.
19	US 20020029359 A1	Method and apparatus for getting dump of a computer system	714/45	Kiyoi, Masahiro et al.
20	US 6535957 B1	System bus read data transfers with bus utilization based data ordering	711/118	Arimilli; Ravi Kumar et al.

	Document ID	Title	Current OR	Inventor
21	US 20050044174 A1	Multi-node computer system where active devices selectively initiate certain transactions using remote-type address packets	709/217	Landin, Anders et al.
22	US 20050005075 A1	Multi-node computer system employing multiple memory response states	711/148	Landin, Anders et al.
23	US 20040215895 A1	Multi-node computer system in which networks in different nodes implement different conveyance modes	711/141	Cypher, Robert E.
24	US 20040002992 A1	Multiprocessing system employing address switches to control mixed broadcast snooping and directory based coherency protocols transparent to active devices	707/102	Cypher, Robert E. et al.
25	US 6877056 B2	System with arbitration scheme supporting virtual address networks and having split ownership and access right coherence mechanism	710/244	Cypher; Robert E.
26	EP 1255201 A1	Shared memory multiprocessing system employing mixed broadcast snooping and directory based coherency protocols		CYPHER, ROBERT et al.

	Document ID	Title	Current OR	Inventor
27	US 20040003181 A1	System with virtual address networks and split ownership and access right coherence mechanism	711/141	Cypher, Robert E.
28	US 20030018739 A1	Shared memory multiprocessing system employing mixed broadcast snooping and directory based coherency protocols	709/213	Cypher, Robert et al.
29	US 20040003183 A1	System with multicast invalidations and split ownership and access right coherence mechanism	711/144	Cypher, Robert E. et al.
30	EP 1376369 A2	System with virtual address networks and split ownership and access right coherence mechanism		CYPHER, ROBERT E
31	US 20050027947 A1	Multi-node computer system including a mechanism to encode node ID of a transaction-initiating node in invalidating proxy address packets	711/148	Landin, Anders
32	US 6457100 B1	Scaleable shared-memory multi-processor computer system having repetitive chip structure with efficient busing and coherence controls	711/119	Ignatowski; Michael et al.
33	US 20050053057 A1	Multiprocessor node controller circuit and method	370/360	Deneroff, Martin M. et al.

	Document ID	Title	Current OR	Inventor
34	US 20030009643 A1	Two-stage request protocol for accessing remote memory data in a NUMA data processing system	711/155	Arimilli, Ravi Kumar et al.
35	US 6810467 B1	Method and apparatus for centralized snoop filtering	711/146	Khare; Manoj et al.
36	US 5966729 A	Snoop filter for use in multiprocessor computer systems	711/146	Phelps; Andrew E.
37	US 20040117561 A1	Snoop filter bypass	711/146	Quach, Tuan M. et al.